Please replace paragraph 16 with the following rewritten paragraph:

In a further advantageous embodiment of the methods according to the invention, it is provided that an interrupt signal immediately triggers, at the processor, while processing a first task using one instruction word page, the execution of the interrupt second task on the other instruction word memory page whereby after the completion of the interrupted second task, processing of the first task can be resumed using the processing state of the said first task in the one instruction word memory page.

IN THE CLAIMS:

Please amend claims 10, 15 and 19 as follows:

10. (Once Amended) A method for generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

combining said primary instruction words into a sequence of associated program words;

reading an instruction word from a row of said instruction word memory determined by a reading row number;

modifying said read instruction word by substituting an instruction word part with an information part of an associated program word;

writing said modified instruction word part to a row of said instruction word memory determined by a writing row number; and

outputting a completed instruction word to drive said functional units of said processor;

wherein said reading row number and said writing row number are provided by respective reading row and writing row registers, and wherein a number of sequential reading row and writing row numbers are determined by contents of a block length register.

15. (Once Amended) A method for the generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

assembling said primary instruction words into a sequence of associated program words;

reading an instruction word from a row and page of said instruction word memory determined by a reading row number and a page number stored in a page register;

modifying said instruction word by substituting an instruction word part with an information part of an associated program word;

writing said modified instruction word to a row and page of said instruction word memory determined by a writing row number and a page number stored in said page register; and

outputting a completed instruction word to control said functional units of said processor.

19. (Once Amended) The improvement specified in claim 18 wherein said address generation unit includes a read pointer register, an associated read pointer up/down counter, a

write pointer register and an associated write pointer up/down counter, wherein said counters provide ring counting in accordance with the contents of a block length register.